REMARKS

Claims 17-19, 21, 24-27 and 31 are the subject of the Office Action. Claims 17, 18 and 27 are amended herein. New claims 32-35 are added.

Claims 17-19, 21, 27 and 31 are rejected as obvious over Ryan in view of Lang et al. Applicant re-emphasizes that Ryan and Lang et al are directed to different fields of endeavor, and both of the references are directed to a field of endeavor different than that to which the present invention is directed.

Ryan describes a transport decoder system, designed for decoding a single transport data stream, as defined by MPEG-2 standards, which includes multiple packetized elementary stream (PES) packets, each having a predetermined synchronization pattern and a predetermined number of bytes, coupled to an NRSS Smart Card that decrypts at least part of the transport data stream (see col. 2, lines 25). The problem faced by Ryan is processing these multiple PES packets in a manner that assures proper synchronization for effective decryption by the NRSS Card. As noted by the Examiner, Ryan teaches a method wherein the transport stream is parsed to derive multiple elementary streams each having an associated program identifier (PID), the PID is used to assign each stream a DMA channel, which in turn is associated with a specific location in the memory of a host computer so that transfers of the multiple elementary streams can be made to corresponding locations in the host computer memory using the DMA channels.

In contrast, Lang et al relates to a multi-channel encoder/decoder for encoding and decoding data communicated over multiple data links each using a data link control protocol such as High-Level Data Link Control (HDLC). The problem faced by Lang et al is processing data streams from a plurality of data links having different interface rates and a multiplicity of possible channelized and unchannelized configurations in a manner that does not place an unacceptably high burden of work on a microprocessor controlling the device. Accordingly, the decoder taught by Lang et al processes multiple data streams, each comprising HDLC packets from one of the physical data links grouped as a data segment. Each incoming data segment is assigned a channel by a channel assigner circuit, pipelined to a time-slice data processor for

decoding, and buffered into channel FIFO buffers according to the channel assigned to the data segment. To accomplish this, a plurality of data packet descriptors are maintained, each referencing a first host memory block capable of holding one of the pipelined data segments stored in the channel FIFO buffers. The data segments are transferred from the channel FIFO buffers via a data bus to the first memory blocks using the data packet descriptors. (see, e.g. col. 6, line 48 - col. 7, line 15).

The Examiner attempts to establish a prima facie case of obviousness by combining Ryan with Lang et al. The Examiner acknowledges that a teaching, suggestion or motivation in the references is required to combine references, and apparently cites Ryan's teaching that allocation for DMA channels is provided in local memory (Flow Control Unit 318). However, the Examiner does not explain why one skilled in the art would look to the Lang et al reference. As applicant has previously argued, one skilled in the art with the knowledge of Ryan would not be motivated to combine the teachings of Ryan and Lang et al because Lang et al relates to the processing of multiple data streams, each comprising HDLC packets, whereas Ryan relates to the processing of a single data stream that has been parsed into multiple PES packets. Lang et al is not in the same field of endeavor, even though it relates generally to computer memories. See, for example, Wang Laboratories, Inc. v Toshiba Corp, 993 F 2d 858, 26 USPQ 2d 1767 (Fed. Cir. 1993). In addition, Lang et al is not reasonably pertinent to the specific problem to which the present invention is concerned, i.e. processing a single transport stream into multiple elemental streams and transferring those streams to the memory of a host computer. It has long been held that such reliance on non-analogous art by the Examiner to establish obviousness is improper. See, e.g. In re Wood, 599 F 2d 1032, 202 USPQ 171 (CCPA 1979).

It is clear from the Examiner's statement on page 5 of the Office Action that the combination of Ryan and Lang does not result in the claimed invention:

> "Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Ryan with Lang, so to provide a method of communicating between a multi-channel network device and a host having host memory with associated buffers for supporting a large number of data links operating at high

speeds due to unacceptably high burden of work placed on the microprocessor (emphasis added)."

As described above, the present invention is directed to methods and devices for processing a single transport stream into multiple elemental streams and transferring those streams to the memory of a host computer, not for "supporting a large number of data links".

As shown in Fig. 3, Lang et al teach a channel assigner (20) that assigns a channel to each incoming data segment, which is processed by a HDLC processor (22) and placed into a FIFO buffer corresponding to its assigned channel. A DMA Controller (24) fetches a partial packet from its FIFO buffer and delivers it into host packet memory. The DMA controller is not directly connected to the host memory PCI bus (as in the present invention - see Fig. 1), rather, memory accesses are serviced by downstream PCI controller (26). DMA Controller communicates with the host using "packet descriptors" ("RPDs"), which are used to manage the transfer of data packets to the host.

The single type of RPDs described by Lang et al is not analogous to the two types of data descriptors taught by the present invention, i.e. frame descriptors and channel context descriptors. For example, the RPDs described in Lang et al only contain the size and location of data buffers in host memory and the data packet information associated with the data in each of those buffers. (See, e.g. col. 17, lines 54-56). Lang et al does not teach or suggest the frame descriptors of the present invention that associates a region in local memory that is the source of data (e.g. local-memory frame descriptor 210 in Fig. 2). As set forth in amended claim 18, when transfers between local memory and host memory are made, local-memory data descriptors associate the data source in local memory and are used in combination with PCI (host) descriptors (e.g. PCI frame descriptor 212 and PCI channel context descriptor 208 in Fig. 2), which associate the data destination in PCI host memory.

In order to more distinctly claim the above-described aspect of the invention, independent claims 17 and 27 have been amended to specify these specific types of data descriptors. New claims 32-35 have been added to specifically define the fields included in each type of data descriptors. Neither Ryan nor Lang teach or describe these specific data descriptors.

Accordingly, it would not have been obvious for one skilled in the art to use the specific data descriptors of the amended claims from a combination of the teachings of Ryan regarding the transfers of multiple elementary streams from local memory and host memory with the teachings of Lang et al regarding the use of single type of RPDs. Reconsideration and withdrawal of the rejection is respectfully requested.

Claims 24-26 are rejected as being obvious over Ryan in view of Lang et al further in view of Fuji et al. As argued above, a combination of Ryan and Lang et al does not teach or suggest the claimed invention. Therefore, modifying Ryan and Lang et al by integrating a network interface connected to a networked computer, as taught by Fuji et al, does not establish that the present invention is obvious. For this reason, reconsideration and withdrawal of the rejection is respectfully requested.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 303-571-4000.

Respectfully submitted,

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